REMARKS/ARGUMENTS

In the Final Office Action mailed November 26, 2008, claims 1, 2, 4, 5, 7, 9, and 10 were rejected. In response, Applicant proposes amending claims 1, 2, and 9 and adding claims 11-13. Applicant respectfully requests that the amendments be entered to put the claims in condition for allowance or to put the claims in better condition for appeal. Applicant hereby requests reconsideration of the application in view of the proposed amendments and the below-provided remarks.

Claim Rejections under 35 U.S.C. 103

Claims 1, 2, 4, 5, 7, 9, and 10 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Hashimoto et al. (U.S. Pat. No. 5,587,962, hereinafter "Hashimoto") in view of Hackett et al. (U.S. Pat. No. 5,585,863, hereinafter "Hackett"). However, Applicant respectfully submits that the pending claims are patentable over Hashimoto and Hackett for the reasons provided below.

Independent Claim 1

Applicant proposes amending claim 1 to include the phrase "that are read out by a line counter" and the phrase "using an adder," and to replace the term "pixel counting means" with the term "a pixel counter." Support for the proposed amendment to claim 1 can be found in Applicant's specification at, for example, Fig. 1 and page 4, lines 22-32. As amended, claim 1 recites:

> "Method of operating a driving circuit for a display system, wherein the sequence of writing and/or reading video data into and/or from a memory is controlled by means of an address sequencer, each of the memory addresses for said video data generated in the address sequencer being composed of a picture line address part or line pointer and an address part for a pixel on said picture line, the method comprising:
>
> operating the driving circuit alternately in a first mode wherein the address sequencer generates addresses for the video data in the memory by combining line pointers that are read out by a line counter from a block of line pointers in address table register means with the output of a pixel counter using an adder, and in a second mode wherein a block of line pointers from a full table of line pointers in said memory is downloaded into said address table register means." (emphasis added)

Hashimoto fails to teach that "*the address sequencer generates addresses for the video data in the memory by combining line pointers that are read out by a line counter*

from a block of line pointers in address table register means with the output of a pixel counter using an adder" (emphasis added), as recited in claim 1.

The Final Office Action states that "Hashimoto does not teach that in the random access mode data addresses are generated by combining line pointers with pixel count." Applicant respectfully agrees. Hashimoto teaches that a pixel address, such as an address of a pixel located at row i column m, may be loaded into a read address buffer register (36b), see Fig. 1 and column 6, lines 59-62. That is, Hashimoto teaches that a location of a pixel at a line can be used as a pixel address. However, Hashimoto fails to teach determining the location of a pixel at a line. In particular, Hashimoto fails to teach directly counting pixels using a pixel counter to determine the location of a pixel at a line.

Hashimoto also fails to teach that lines pointers are read out by a line counter. Hashimoto teaches column numbers and row numbers of a frame (10), see Fig. 1 and column 6, lines 59-67. However, Hashimoto fails to teach that the column numbers and the row numbers of the frame (10) are read out by directly counting lines of the frame (10).

Additionally, Hashimoto fails to teach that a memory address is the result of combining a line count and a pixel count using an adder. Hashimoto teaches that an address corresponding to a pixel located at row i+1 and column m may be loaded into an address buffer register (36b) and transferred to an address sequencer (40b), see Fig. 2 and column 7, lines 1-6. However, Hashimoto fails to teach that the address corresponding to the pixel located at row i+1 and column m is the result of combining the column number i+1 and the row number m using an adder.

Thus, Hashimoto fails to teach that "*the address sequencer generates addresses for the video data in the memory by combining line pointers that are read out by a line counter from a block of line pointers in address table register means with the output of a pixel counter using an adder*" (emphasis added), as recited in claim 1. Accordingly, Hashimoto and Hackett fail to teach all the limitations of amended claim 1. As a result, Applicant respectfully asserts that amended claim 1 is not rendered obvious over Hashimoto in view of Hackett.

Independent Claim 2

Applicant proposes amending claim 2 to include the phrase "that are read out by a line counter" and the phrase "using an adder," and to replace the term "pixel counting means" with the term "a pixel counter." Support for the proposed amendment to claim 2 can be found in Applicant's specification at, for example, Fig. 1 and page 4, lines 22-32. As amended, claim 2 includes similar limitations to amended claim 1. Because of the similarities between claim 1 and claim 2, Applicant respectfully asserts that the remarks provided above with regard to amended claim 1 apply also to amended claim 2. Accordingly, Applicant respectfully asserts that amended claim 2 is patentable over Hashimoto in view of Hackett.

Dependent Claims 4, 5, 7, and 10

Claims 4, 5, 7, and 10 depend from and incorporate all of the limitations of the independent claim 2. Applicant respectfully asserts that claims 4, 5, 7, and 10 are allowable at least based on an allowable claim 2.

Independent Claim 9

Applicant proposes amending claim 9 to include the phrase "that are read out by a line counter" and the phrase "using an adder," and to replace the term "pixel counting means" with the term "a pixel counter." Support for the proposed amendment to claim 9 can be found in Applicant's specification at, for example, Fig. 1 and page 4, lines 22-32. As amended, claim 9 includes similar limitations to amended claim 1. Because of the similarities between claim 1 and claim 9, Applicant respectfully asserts that the remarks provided above with regard to amended claim 1 apply also to amended claim 9. Accordingly, Applicant respectfully asserts that amended claim 9 is patentable over Hashimoto in view of Hackett.

New Claims 11-13

Applicant proposes adding new claims 11-13. Support for claims 11-13 can be found in Applicant's specification at, for example, page 5, lines 2-4. Claim 11 depends from and incorporates all of the limitations of the independent claim 1. Claim 12

depends from and incorporates all of the limitations of the independent claim 2. Claim 13 depends from and incorporates all of the limitations of the independent claim 9. Thus, Applicant respectfully asserts that claims 11-13 are allowable at least based on allowable claims 1, 2, and 9 respectively. Additionally, claims 11-13 may be allowable for further reasons, as described below.

Hackett fails to teach "*wherein each block of line pointers is limited to thirty two line pointers*" (emphasis added), as recited in claim 11. Hackett teaches creating a line pointer table using a block of lines, sees column 2, lines 63-66 and column 3, lines 15-20. However, Hackett fails to teach that the block of lines is limited to thirty two lines. Additionally, Hackett fails to teach "*wherein the number of line pointers in the address table register means is limited to thirty two,*" as recited in claims 12 and 13.

CONCLUSION

Applicant respectfully requests reconsideration of the claims in view of the proposed amendments and remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,

/mark a. wilson/

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Mark A. Wilson
Reg. No. 43,994

Wilson & Ham
PMB: 348
2530 Berryessa Road
San Jose, CA 95132
Phone: (925) 249-1300
Fax: (925) 249-0111